

FIG. 1

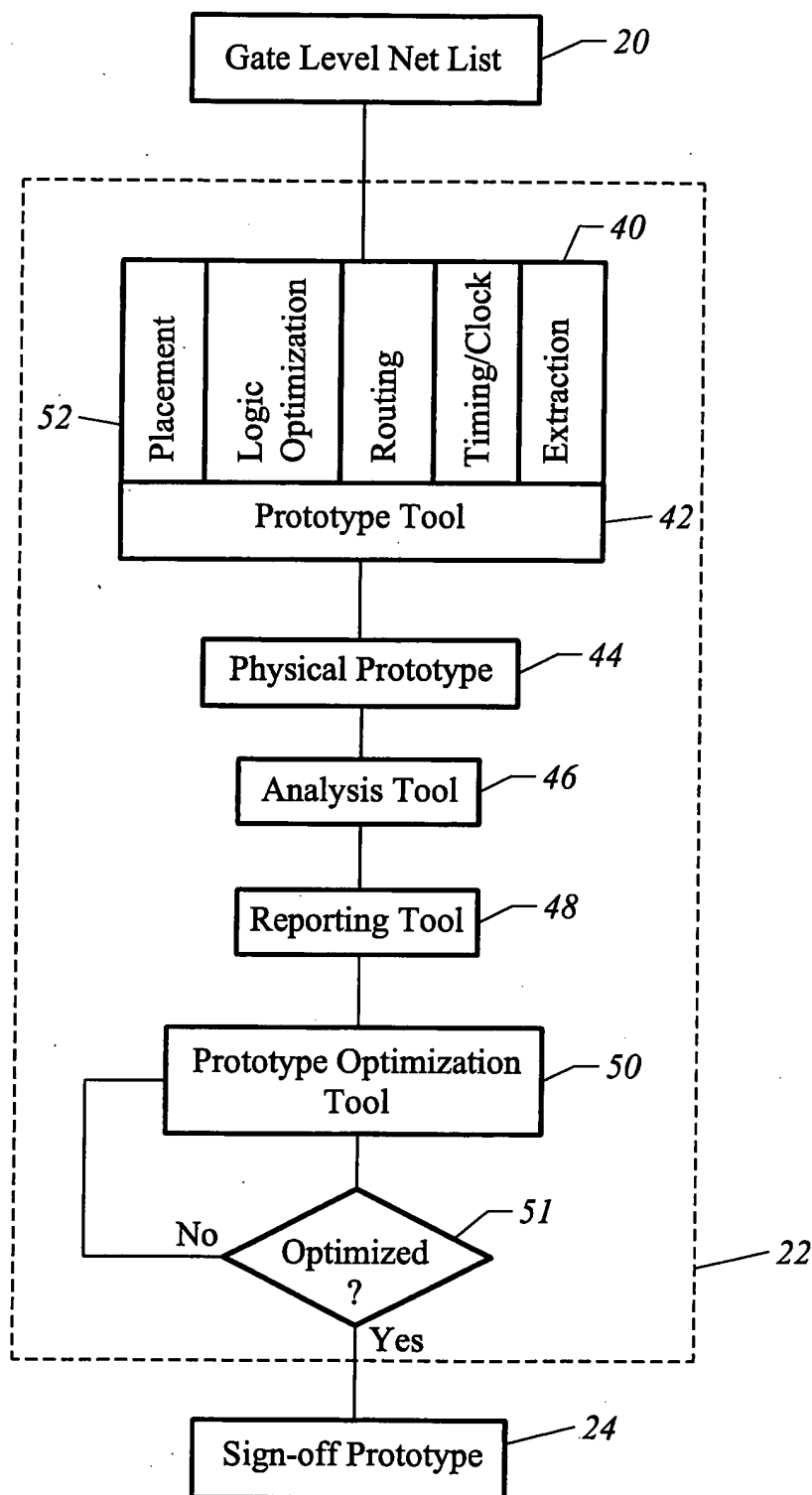


FIG. 2

Title: Method and Apparatus for Generating Sign-Off Prototypes for the Design and Fabrication of Integrated Circuits

Applicants: Raje, et al.
Appl. No.: 09/632,494
Filing Date: August 3, 2000

Docket: MONT-01307US0
Atty: Burt Magen
Phone: (415) 369-9660

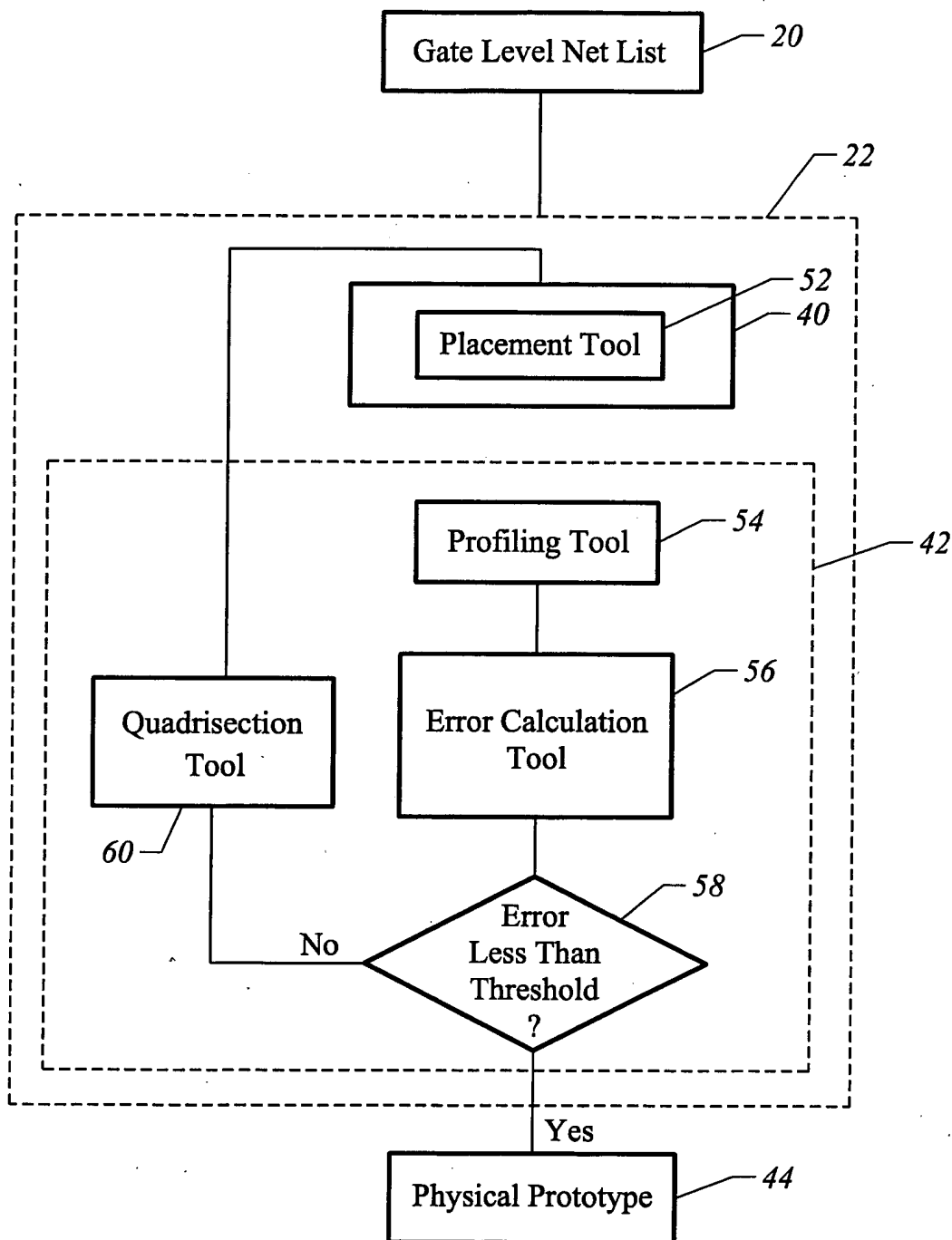
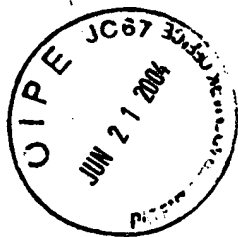


FIG. 3



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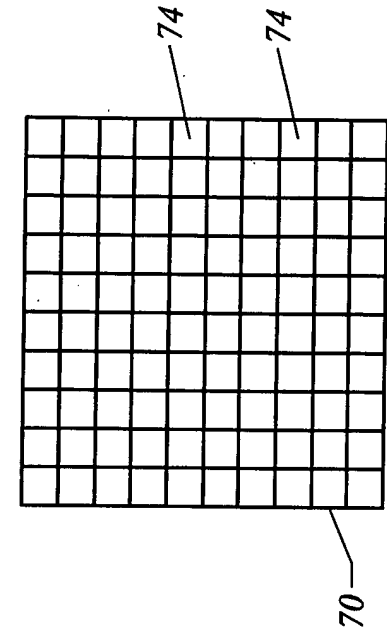


FIG. 4A

instances
of net

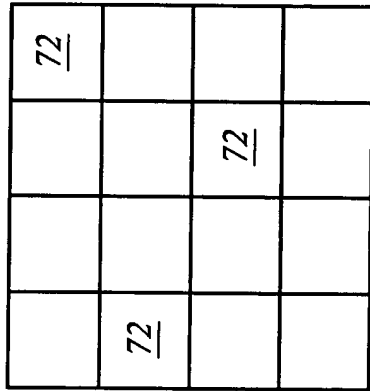


FIG. 4B

instances
of net

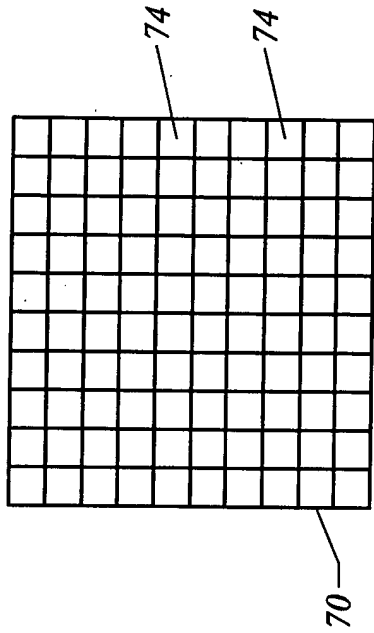


FIG. 4C

instances
of net

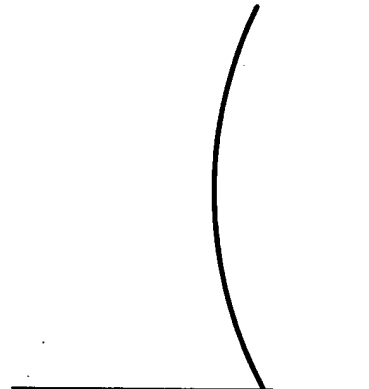


FIG. 5A

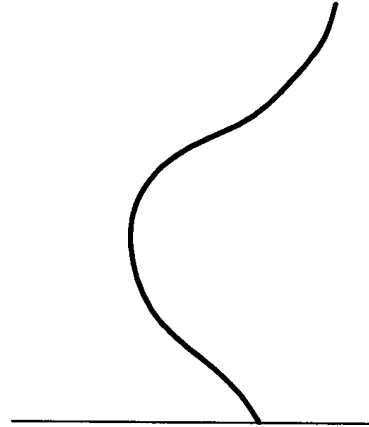


FIG. 5B

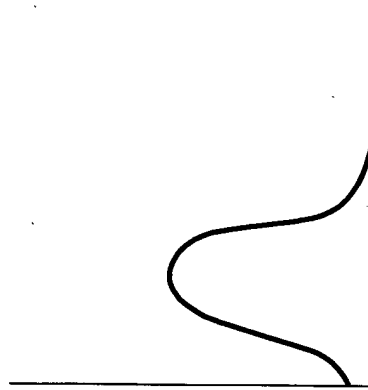


FIG. 5C



Title: Method and Apparatus for Generating Sign-Off Prototypes for the Design and Fabrication of Integrated Circuits

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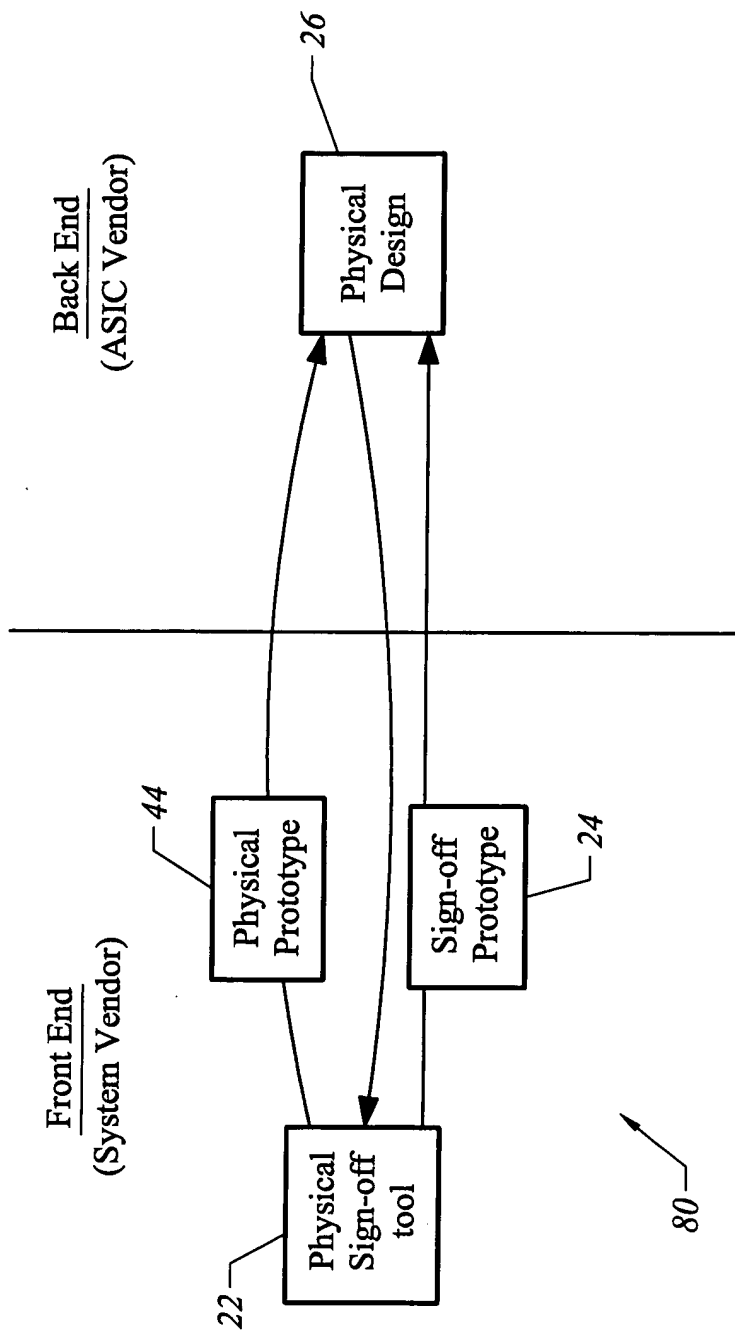


FIG. 6



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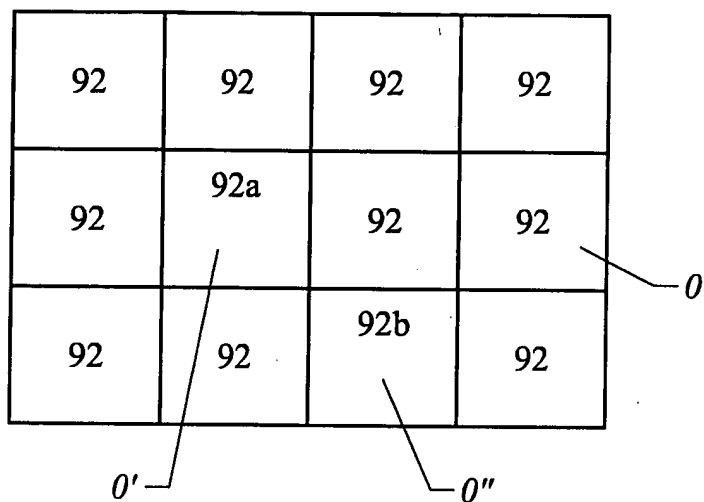


FIG. 7

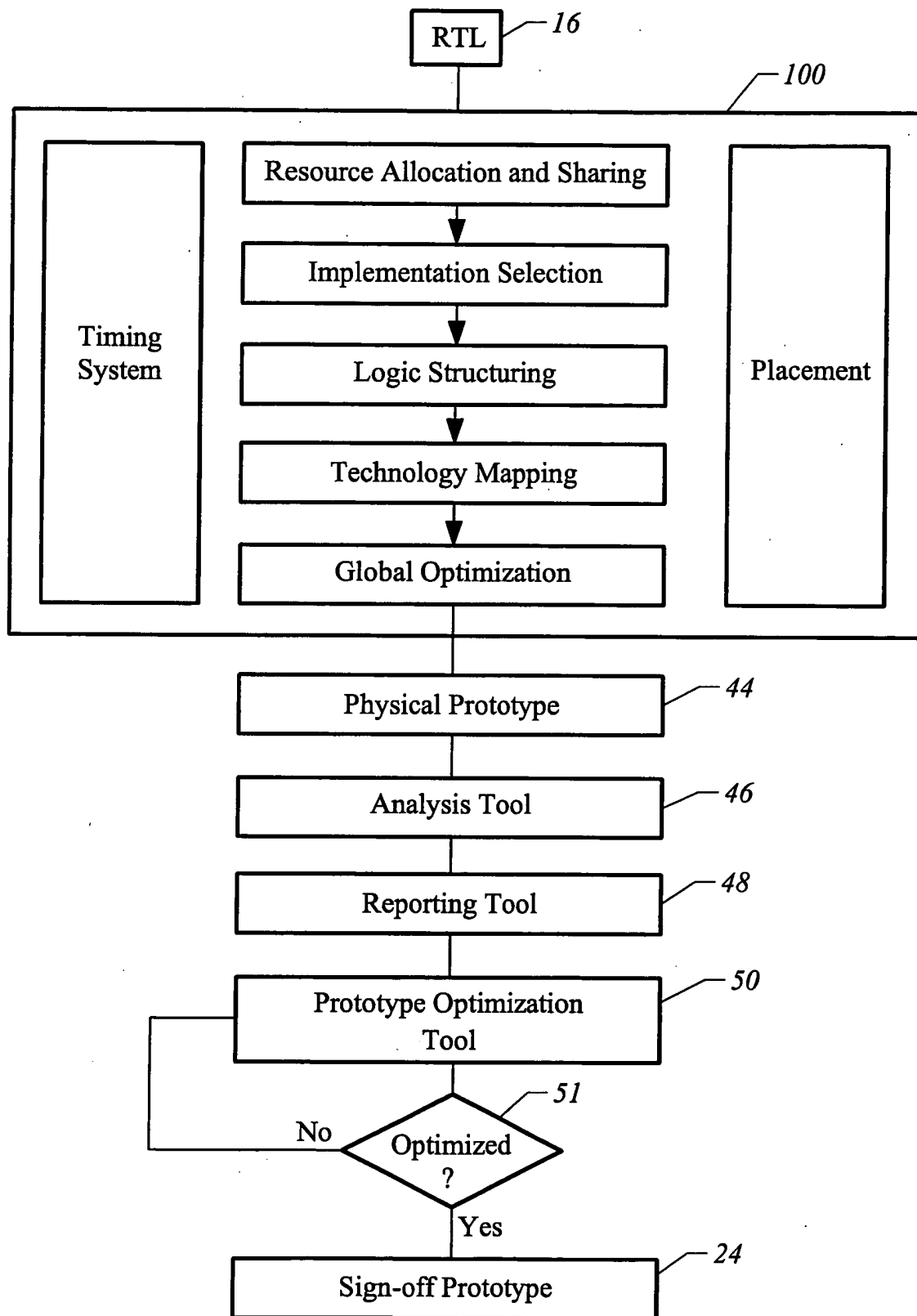


FIG. 8

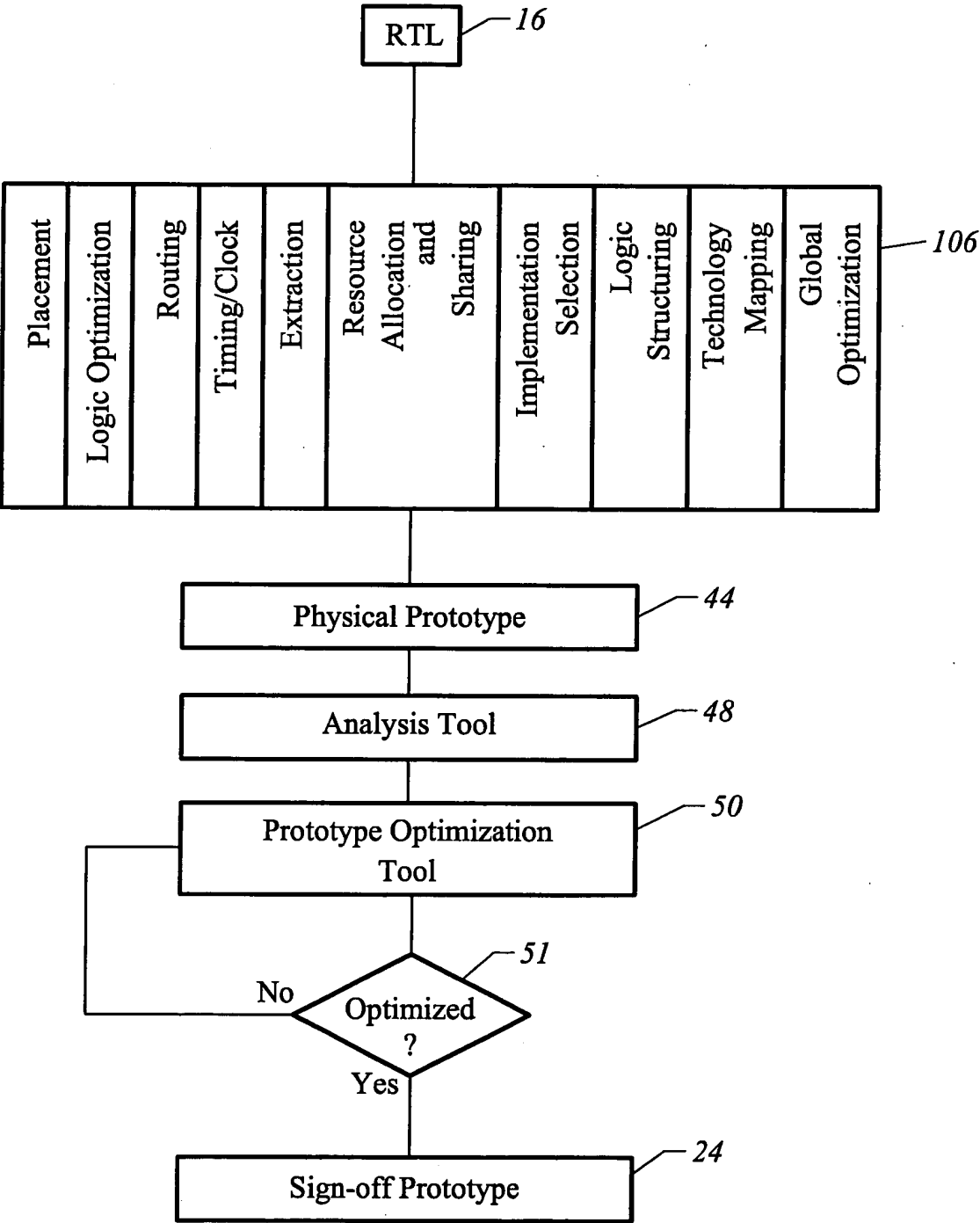


FIG. 9